IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Fereidoon Heydari and Hakan Ozdemir
Title:	DATA CODE AND METHOD FOR CODING DATA
Serial No.:	09/994,009
Filing Date:	November 5, 2001
Examiner/Unit:	Glenda P. Rodriguez/2651
Attorney Docket No.:	01-S-023 (1678-39)

CERTIFICATE OF MAILING OR TRANSMISSION

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Kelly Pedersen
(Signature)

REASONS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

In accordance with the Pre-Appeal Brief Request for Review, Applicants submit the following:

Claims 1-30 and 32-34 are pending, and are rejected under 35 U.S.C. § 102(b) in view of U.S. 5,661,760 to Patapoutian.

The application is currently under final rejection (final Office Action mailed 26 October 2006).

The Applicants' attorney is requesting review of the claims as listed in the response (mailed 02 August 2006) to the non-final Office Action mailed 02 May 2006.

The Examiner and Applicants' attorney had scheduled a telephone interview for 17 January 2007.

But due to a previously scheduled CLE class that did not appear on the attorney's calendar, on 15 or 16 January 2007 the attorney left the Examiner a voice mail cancelling the telephone interview and requesting that the Examiner phone the attorney to reschedule the interview. During the following three weeks, the attorney left for the Examiner three additional voice mails requesting a rescheduling of the interview. The Examiner never responded to any of these voice mails.

Claim 1 of the patent application as currently pending is directed to a coded binary sequence comprising first and second groups of consecutive bits.

E.g., Table I (paragraph [25]) and FIG. 5 of the patent application disclose an embodiment of the first group of consecutive bits recited in claim 1. Specifically, Table I and FIG. 5 disclose a first group of consecutive bits (0011), the first group having first (00) and second (11) separate portions (50a and 50b in FIG. 5) and representing one of a logic 1 and a logic 0 (in this embodiment 0011 represents a logic 1), the bits in the first portion each having a first state (both bits have state 0 in this embodiment) and the bits in the second portion each having a second state (both bits have state 1 in this embodiment). Table II (paragraph [33]) discloses another embodiment of the first group of consecutive bits.

The Applicants' attorney does not dispute that U.S. 5,661,760 to Patapoutian anticipates the first group of consecutive bits as recited in claim 1. Referring, *e.g.,* to col. 3, lines 55-58, Patapoutian discloses representing a binary zero (*i.e.,* a logic 0) as ++-- and representing a binary one (*i.e.,* a logic 1) as --++, where "-" represents a first

biphase magnetization state, *i.e.*, polarity, and where "+" represents a second biphase magnetization state.

E.g., Table I (paragraph [25]) and FIG. 5 of the patent application also disclose an embodiment of the second group of consecutive bits recited in claim 1. Specifically, Table I and FIG. 5 disclose a second group of consecutive bits (0000) separate from the first group [of bits (0011)] and each having a same state (each bit in the second group has the same state 0), the second group representing only the other of the logic 1 and logic 0 (in this embodiment, because the first group of bits 0011 represents a logic 1, the second group of bits 0000 represents only a logic 0). Table II (paragraph [33]) discloses another embodiment of the second group of consecutive bits.

But unlike the first group of consecutive bits, Patapoutian does not anticipate the second group of consecutive bits as recited in claim 1. Referring, *e.g.*, to col. 3, lines 55-58, Patapoutian discloses representing a logic 0 as "++--"; but, unlike the claimed second group of consecutive bits, these magnetizations do not each have the same state (polarity). That is, the first two magnetizations have the same state "+", but the second two magnetizations have a different state "-". For Patapoutian to anticipate the second group of consecutive bits, he would need to have disclosed representing a logic 0 or logic 1 with a sequence of all "-" states (*e.g.*, "----") or a sequence of all "+" states (*e.g.*, "++++").

Referring to page 2 of the final Office Action mailed 26 October 2006, as best understood by the Applicants' attorney, the Examiner is interpreting the term "bit" in claim 1 in a manner that is inconsistent with the plain and intended meaning of "bit". Specifically, the Examiner is trying to read the claim term "bit" on a group of multiple "bits".

The Examiner argues, for example, that coding a sequence of two logic 0's (i.e., 00) according to Patapoutian's scheme results in the sequence ++--++-- of magnetizations, and the Examiner views this sequence as including a first magnetization pattern ++-- followed by an identical second magnetization pattern ++--.

By viewing each of the first and second magnetization patterns as a single entity and not as comprising multiple magnetizations, the Examiner concludes that each of the first and second magnetization patterns has the same state.

Therefore, according to the Examiner, Patapoutian's coding (++--++--) of a sequence of two logic 0's (00) anticipates "the second group of consecutive bits" recited in claim 1 because each of Patapoutian's first and second magnetization patterns (++--) is equivalent to a "bit", and each of Patapoutian's "bits" has the same state (++--).

But the Examiner's interpretation of "bit" is inconsistent with the plain and intended meaning of "bit".

"Bit" is short for "binary digit", which is a digit having one of only two possible values, *e.g.,* 0 or 1. But when viewed as a single entity, a group of bits is not and cannot be a bit because the group has one of more than two possible values. For example, a group of two bits has one of four possible values.

Because Patapoutian's magnetizations have only two possible states (polarizations) "-" and "+", each of these magnetizations (and not groups of these magnetizations as argued by the Examiner) is equivalent to a "bit" as recited in claim 1.

Therefore, it follows that a group of Patapoutian's magnetizations (*e.g.,* --++) is equivalent to a group of bits, and not to a "bit" as recited in claim 1.

In summary, the term "bit" as recited in claim 1 reads on a single one of Patapoutian's magnetizations (+ or -), but does not read on a group (*e.g.,* --++) of these magnetizations.

Consequently, the proper analysis is to compare the "second group of consecutive bits" recited in claim 1 to each of Patapoutian's magnetization patterns ++-- (logic 0) and --++ (logic 1) separately, and not view these patterns a "bits" that compose the "second group of consecutive bits".

But as stated above, under this analysis neither of Patapoutian's magnetization patterns ++-- and --++ anticipates the "second group of consecutive bits" as recited in claim 1. The magnetizations composing the pattern ++-- do not each have the same state (polarity). That is, these magnetizations have different states, *i.e.,* the first two

magnetizations have a "+" state, and the last two magnetizations have a "-" state. Similarly, the magnetizations composing the pattern ++-- do not each have the same state (polarity).

The other claims 2-30 and 32-34 are patentable for generally similar reasons.

Consequently, in light of the above, all of the claims are in condition for allowance over the cited prior art.

In the event additional fees are due, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

DATED this 26th day of March, 2007.

Respectfully submitted,

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